C: Remarks:

Notice of Non-Compliant Amendment dated 8/30/2007

Applicants respectfully request entry of the following corrected amendment which underlines processor in line 11 of claim 1.

The present amendment is filed formally in accordance with the examiner's suggestions which are appreciated and to place this application in condition for allowance. The examiner is thanked for the suggestions.

Morioka et al (6,631,447) attempted to achieve benefits that the applicant's claimed invention solved, but has limitations which requred manipulation of page table information that is cached in the TLB.

The claimed invention was focused on using the dispatch of virtual processors for controlling the size and extent of a required coherency domain. Claim 1 now recites "to determine which coherent cache regions in the system are required to examine a coherency transaction produced by a storage request of a single originating processor of said computer system and to change coherency boundaries directly with coherency mode bits" (See claim 1 as amended).

Morioka did not teach the use of virtual processor dispatch (see new claim 16) and focused only on manipulation of page table information that is cached in the TLB. Morioka detailed description does not give any indication that they foresaw the claimed use of the virtual processor management to more efficiently control the cache coherency domains. This invention is much more direct, the control program can change the coherency boundaries directly by changing our "Coherency Mode Bits" which is claimed in claim 1, with futher specifics in dependent claims. The claimed invention does not require the intermediate steps of changing page tables and manipulating TLB entries.

Morioka limitations:

They use TLB to hold the information which defines whether an address requires a global coherency search.

- the applicants' claimed invention does not use the TLB for this function (much less hardware area is required)

- since Morioka uses the TLB it needs to modify hundreds or thousands of TLB entries when the coherence boundaries are dynamically changed.

They use Page Table Entries (PTE) to hold the same information (LCC/GCC). This requires a larger PTE, our invention does not require this.

Figure 5 of Morioka clearly shows the limitation of that earlier patent. The LCC/GCC determination comes from the TLB. The Cluster ID No (311) is static, there is no indication in Morioka that the Cluster ID number would be changed after an initial setup.
This patent application shows how to have an adjustable system. Putting the LCC/GCC indication in the TLB entries makes adjustments difficult, while this application's solution is different and better.

Take the Morioka example of changing a partition from LCC to GCC as the processing needs for that partition grows. In the applicants' invention they simply dispatch the workload with the wider scope (see page 4 paragraph 37). The same change of coherency boundaries using Morioka requires change to the page table settings and selective purging/updating of the TL Bs.

As to the second grounds of rejection. The Hagersten patent that the examiner points to (6226671) seems not to have a figure 2 with elements 30A and 30B which the examiner used as the reason for his rejection.. Thus the claims are not understood. Clarification is requested. Nevertheless, the claims have been amended, so a new reconsideration of Hagersten 6226671 is required, as Hagersten does not " determine which coherent cache regions in the system are required to examine a coherency transaction produced by a storage request of a single originating processor of said computer system and to change coherency boundaries directly with coherency mode bits ".

A notice of allowance is respectfully requested.

RESPECTFULLY SUBMITTED
(For the inventors)
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